Department of Electronics and Communication Engineering

Assignment -1

Total marks-10

Branch:B Tech ECE

Subject & Subject code: Digital System Design and BTEC– 302

Semester: 3rd
Date on which assignment is given: 20.8.24 **Date of submission of assignment: 27.8.24**

Course Outcomes:

CO 1	Apply concepts of Boolean algebra for handling logical expressions.
CO 2	Apply working and realization of combinational logical expressions.
CO 3	Realize working flip-flops and use them in designing of sequential circuits.
CO 4	Apply fundamental concepts of logic families and architectural of programmable devices.
CO 5	Use HDL programming tool for simulation of combinational and sequential circuits

Bloom's Taxonomy Levels

L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analyzing, L5 – Evaluating, L6 - Creating

S. No.	Questions	Marks	Relevance to CO No.	Bloom's Level
1.	a) Design the Half adder using 4:1 mux. b) Minimize the following Boolean function using K-map $F(A,B,C,D) = \sum (4,5,6,7,12,13,14) + d(1,9,11,15)$	2	CO2	L5
2.	Implement the 4 bit binary to gray code convertor (using K-map for each output).	2	CO2	L3
3.	(a) Define Decoder. Design 3 to 8 line Decoder. (b) Design & implement a Full Adder using Decoder and two OR gates	2	CO2	L3
4.	Convert the following. (a) $(BC)_{16} = (\ )_{10}$ (b) $(2314)_8 == (\ )_{16}$; $= (\ )_{10}$	2	CO1	L2

5.	Simplify the following Boolean functions to minimum number of literals. i) F=xy+x'z+yz. ii) F=x'y'z+x'yz+xy'	2	CO 1	L1